WHAT IS CLAIMED IS:

1. An electronic device comprising a plurality of pixels, wherein each of the plurality of pixels has a plurality of memory circuits and a plurality of non-volatile memory circuits.

2. A device according to claim 1, wherein the memory circuits are static memories (SRAMs).

3. A device according to claim 1, wherein the memory circuits are ferroelectric memories (FeRAMs).

4. A device according to claim 1, wherein the memory circuits are dynamic memories (DRAMs).

5. A device according to claim 1, wherein the non-volatile memory circuits are electrically writable, readable, and erasable non-volatile memories (EEPROMs).

6. A device according to claim 1, wherein the memory circuits are formed over a glass substrate.

7. A device according to claim 1, wherein the memory circuits are formed over a plastic substrate.

8. A device according to claim 1, wherein the memory circuits

are formed over a stainless steel substrate.

9. A device according to claim 1, wherein the memory circuits are formed on a single crystal wafer.

10. Electronic equipment employing the electronic device according to claim 1.

11. An electronic device comprising a plurality of pixels, wherein:

each of the plurality of pixels has n x m memory circuits for storing m frame portions (where m is a natural number, $m \geq 1$) of an n-bit digital image signal (where n is a natural number, $n \geq 2$); and

each of the plurality of pixels has n x k non-volatile memory circuits for storing k frame portions (where k is a natural number, $k \geq 1$) of the n-bit digital image signal.

12. A device according to claim 11, wherein the memory circuits are static memories (SRAMs).

13. A device according to claim 11, wherein the memory circuits are ferroelectric memories (FeRAMs).

14. A device according to claim 11, wherein the memory circuits are dynamic memories (DRAMs).

15. A device according to claim 11, wherein the non-volatile memory circuits are electrically writable, readable, and erasable non-volatile memories (EEPROMs).

16. A device according to claim 11, wherein the memory circuits are formed over a glass substrate.

17. A device according to claim 11, wherein the memory circuits are formed over a plastic substrate.

18. A device according to claim 11, wherein the memory circuits are formed over a stainless steel substrate.

19. A device according to claim 11, wherein the memory circuits are formed on a single crystal wafer.

20. Electronic equipment employing the electronic device according to claim 11.

21. An electronic device comprising a plurality of pixels, each of the pixels having:

a source signal line;

n (where n is a natural number, $n \geq 2$) gate signal lines used for write-in;

n gate signal lines used for read-out;

n transistors used for write-in;

n transistors used for read-out;

n x m memory circuits for storing m frame portions (where m is a natural number, $m \geq 1$) of an n-bit digital image signal;

n x k non-volatile memory circuits for storing k frame portions (where k is a natural number, $k \geq 1$) of the n-bit digital image signal;

2n memory circuit selection portions;

2n non-volatile memory circuit selection portions;

an electric current supply line;

an EL driver transistor; and

an EL element;

wherein:

gate electrodes of the n write-in transistors are each electrically connected to any one of the n write-in gate signal lines, with each of said gate electrodes connected to a different write-in gate signal line;

input electrodes of the n write-in transistors are each electrically connected to the source signal line;

output electrodes of the n write-in transistors are electrically connected to the m memory circuits through any one of the n memory circuit selection portions, with each of said output electrodes connected through a different memory circuit selection portion;

the output electrodes of the n write-in transistors are electrically connected to the k non-volatile memory circuits through any one of the n memory circuit selection portions, with each of said output electrodes connected through a different non-volatile memory circuit selection portion;

gate electrodes of the n read-out transistors are each electrically connected to any one of the n read-out gate signal lines, with each of said gate electrodes connected to a different read-out gate signal line;

the input electrodes of the n write-in transistors are electrically connected to the k non-volatile memory circuits through any one of the n memory circuit selection portions, with each of said input electrodes connected through a different memory circuit selection portion;

the input electrodes of the n write-in transistors are electrically connected to the k non-volatile memory circuits through any one of the n non-volatile memory circuit selection portions, with each of said input electrodes connected through a different non-volatile selection portion;

the output electrodes of the n write-in transistors are each electrically connected to a gate electrode of the EL driver transistor;

an input electrode of the EL driver transistor is electrically connected to the electric current supply line; and

an output electrode of the EL driver transistor is

electrically connected to one electrode of the EL element.

22. A device according to claim 21, wherein the memory circuits are static memories (SRAMs).

23. A device according to claim 21, wherein the memory circuits are ferroelectric memories (FeRAMs).

24. A device according to claim 21, wherein the memory circuits are dynamic memories (DRAMs).

25. A device according to claim 21, wherein the non-volatile memory circuits are electrically writable, readable, and erasable non-volatile memories (EEPROMs).

26. A device according to claim 21, wherein the memory circuits are formed over a glass substrate.

27. A device according to claim 21, wherein the memory circuits are formed over a plastic substrate.

28. A device according to claim 21, wherein the memory circuits are formed over a stainless steel substrate.

29. A device according to claim 21, wherein the memory circuits

are formed on a single crystal wafer.

30. Electronic equipment employing the electronic device according to claim 21.

31. A device according to claim 21, wherein:

the memory circuit selection portions:

select any one circuit from among the m memory circuits and the k non-volatile memory circuits, make the output electrode of the write-in transistor conductive to the selected one circuit from among the m memory circuits and the k non-volatile memory circuits, and perform write-in of the digital image signal to the selected one circuit; or

select any one circuit from among the m memory circuits and the k non-volatile memory circuits, make the input electrode of the write-in transistor conductive to the selected one circuit from among the m memory circuits and the k non-volatile memory circuits, and perform read-out of the digital image signal from the selected one circuit.

32. A device according to claim 21, wherein the electronic device has:

a shift register for outputting sampling pulses one after another in accordance with a clock signal and a start pulse;

a first latch circuit for storing the n-bit digital image

signal (where n is a natural number, $n \geq 2$) in accordance with the sampling pulse;

a second latch circuit into which the n-bit digital image signal stored in the first latch circuit is transferred; and

a bit selection circuit for selecting, in order, one bit portions of the n-bit digital image signal transferred to the second latch circuit, and outputting to the source signal line.

33. An electronic device comprising a plurality of pixels, each of the pixels having:

n (where n is a natural number, $n \geq 2$) source signal lines;

gate signal lines used for write-in;

n gate signal lines used for read-out;

n transistors used for write-in;

n transistors used for read-out;

n x m memory circuits for storing m frame portions (where m is a natural number, $m \geq 1$) of an n-bit digital image signal;

n x k non-volatile memory circuits for storing k frame portions (where k is a natural number, $k \geq 1$) of the n-bit digital image signal;

2n memory circuit selection portions;

2n non-volatile memory circuit selection portions;

an electric current supply line;

an EL driver transistor; and

an EL element;

wherein:

gate electrodes of the n write-in transistors are each electrically connected to any one of the write-in gate signal lines, with each of said gate electrodes connected to a different write-in gate signal line;

input electrodes of the n write-in transistors are each electrically connected to any one of the sources signal lines, with each of said input electrodes connected to a different source signal line;

output electrodes of the n write-in transistors are electrically connected to m memory circuits through any one of the n memory circuit selection portions, with each of said output electrodes connected through a different memory circuit selection portion;

the output electrodes of the n write-in transistors are electrically connected to the k non-volatile memory circuits through any one of the n non-volatile memory circuit selection portions, with each of said output electrodes connected through a different non-volatile memory circuit selection portion;

gate electrodes of the n read-out transistors are each electrically connected to any one of the n read-out gate signal lines, with each of said gate electrodes connected to a different read-out gate signal line;

input electrodes of the n read-out transistors are

electrically connected to the k non-volatile memory circuits through any one of the n memory circuit selection portions, with each of said input electrodes connected through a different memory circuit selection portion;

the input electrodes of the n read-out transistors are electrically connected to the k non-volatile memory circuits through any one of the n non-volatile memory circuit selection portions, with each of said input electrodes connected through a different non-volatile selection portion;

the output electrodes of the n write-in transistors are each electrically connected to a gate electrode of the EL driver transistor;

an input electrode of the EL driver transistor is electrically connected to the electric current supply line; and

an output electrode of the EL driver transistor is electrically connected to one electrode of the EL element.

34. A device according to claim 33, wherein the memory circuits are static memories (SRAMs).

35. A device according to claim 33, wherein the memory circuits are ferroelectric memories (FeRAMs).

36. A device according to claim 33, wherein the memory circuits are dynamic memories (DRAMs).

37. A device according to claim 33, wherein the non-volatile memory circuits are electrically writable, readable, and erasable non-volatile memories (EEPROMs).

38. A device according to claim 33, wherein the memory circuits are formed over a glass substrate.

39. A device according to claim 33, wherein the memory circuits are formed over a plastic substrate.

40. A device according to claim 33, wherein the memory circuits are formed over a stainless steel substrate.

41. A device according to claim 33, wherein the memory circuits are formed on a single crystal wafer.

42. A device according to claim 33, wherein:

the memory circuit selection portions:

select any one circuit from among the m memory circuits and the k non-volatile memory circuits, make the output electrode of the write-in transistor conductive to the selected one circuit from among the m memory circuits and the k non-volatile memory circuits, and perform write-in of the digital image signal to the selected one circuit; or

select any one circuit from among the m memory circuits and the k non-volatile memory circuits, make the input electrode of the write-in transistor conductive to the selected one circuit from among the m memory circuits and the k non-volatile memory circuits, and perform read-out of the digital image signal from the selected one circuit.

43. A device according to claim 33, wherein the electronic device has:

a shift register for outputting sampling pulses one after another in accordance with a clock signal and a start pulse;

a first latch circuit for storing one bit of the digital image signal from among the n-bit digital image signal (where n is a natural number, $n \geq 2$); and

a second latch circuit into which the one bit of the digital image signal stored in the first latch circuit is transferred, and which outputs the one bit of the digital image signal to the source signal line.

44. A device according to claim 33, wherein the electronic device has:

a shift register for outputting sampling pulses one after another in accordance with a clock signal and a start pulse;

a latch circuit for storing one bit of the digital image signal in accordance with the sampling pulse; and

a bit selection circuit for selecting the source signal line for outputting the one bit of the digital image signal which has been transferred to the latch circuit.

45. Electronic equipment employing the electronic device according to claim 33.

46. A method of driving an electronic device for performing display of an image using an n-bit digital image signal (where n is a natural number, $n \geq 2$), wherein:

the electronic device has a source signal line driver circuit, a gate signal line driver circuit, and a plurality of pixels;

in the source signal line driver circuit: a sampling pulse is output from a shift register and input to a latch circuit; the digital image signal is stored in the latch circuit in accordance with the sampling pulse; and write in of the stored digital image signal to a source signal line is performed;

in the gate signal line driver circuit: a gate signal line selection pulse is output and a gate signal line is selected; and

in the plurality of pixels: in a row in which the gate signal line is selected, write in of the n-bit digital image signal input from the source signal line to a memory circuit; read out of the n-bit digital image signal stored in the memory circuit; write in of the n-bit digital image signal input from the source signal

line, or write in of the n-bit digital image signal stored in the memory circuit, to a non-volatile memory circuit; read out of the n-bit digital image signal stored in the non-volatile memory circuit; or write in of the n-bit digital image signal stored in the non-volatile memory circuit to the memory circuit is performed.

47. A method according to claim 46, wherein:

in a static image display period:

the source signal line driver circuit is stopped by repeatedly reading out the n-bit digital image signal stored in the memory circuit, and performing display of a static image.

48. Electronic equipment employing the method according to claim 46.

49. A method of driving an electronic device for performing display of an image using an n-bit digital image signal (where n is a natural number, $n \geq 2$), wherein:

the electronic device has a source signal line driver circuit, a gate signal line driver circuit, and a plurality of pixels;

in the source signal line driver circuit: a sampling pulse is output from a shift register and input to a latch circuit; the digital image signal is stored in the latch circuit in accordance with the sampling pulse; and write in of the stored digital image signal to a source signal line is performed;

the gate signal line driver circuit outputs a gate signal line selection pulse, and selects gate signal lines in order from a first row; and

in the plurality of pixels: write in of the n-bit digital image signal in order from the first row; or read out of the n-bit digital image signal is performed.

50. A method according to claim 49, wherein:

in a static image display period:

the source signal line driver circuit is stopped by repeatedly reading out the n-bit digital image signal stored in the memory circuit, and performing display of a static image.

51. Electronic equipment employing the method according to claim 49.

52. A method of driving an electronic device for performing display of an image using an n-bit digital image signal (where n is a natural number, $n \geq 2$), wherein:

the electronic device has a source signal line driver circuit, a gate signal line driver circuit, and a plurality of pixels;

in the source signal line driver circuit: a sampling pulse is output from a shift register and input to a latch circuit; the digital image signal is stored in the latch circuit in accordance with the sampling pulse; and write in of the stored digital image

signal to a source signal line is performed;

the gate signal line driver circuit specifies an arbitrary row of gate signal lines and outputs a gate signal line selection pulse; and

in the plurality of pixels: write in of the n-bit digital image signal in the specified arbitrary row of the gate signal lines; or read out of the n-bit digital image signal is performed.

53. A method according to claim 52, wherein:

in a static image display period:

the source signal line driver circuit is stopped by repeatedly reading out the n-bit digital image signal stored in the memory circuit, and performing display of a static image.

54. Electronic equipment employing the method according to claim 52.

55. Electronic equipment according to claim 10, wherein the electronic equipment is at least one selected from the group consisting of: a television, a personal computer, a portable terminal, a video camera, and a head mounted display.

56. Electronic equipment according to claim 20, wherein the electronic equipment is at least one selected from the group consisting of: a television, a personal computer, a portable terminal,

a video camera, and a head mounted display.

57. Electronic equipment according to claim 30, wherein the electronic equipment is at least one selected from the group consisting of: a television, a personal computer, a portable terminal, a video camera, and a head mounted display.

58. Electronic equipment according to claim 45, wherein the electronic equipment is at least one selected from the group consisting of: a television, a personal computer, a portable terminal, a video camera, and a head mounted display.

59. Electronic equipment according to claim 48, wherein the electronic equipment is at least one selected from the group consisting of: a television, a personal computer, a portable terminal, a video camera, and a head mounted display.

60. Electronic equipment according to claim 51, wherein the electronic equipment is at least one selected from the group consisting of: a television, a personal computer, a portable terminal, a video camera, and a head mounted display.

61. Electronic equipment according to claim 54, wherein the electronic equipment is at least one selected from the group consisting of: a television, a personal computer, a portable terminal, a video camera, and a head mounted display.